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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Number	10/684348	**Docket Number**	MIPS.0189-00-US
Filed	10/10/2003	**Group Art Unit**	
Examiner		**Customer No.**	23669
Application Title	INTEGRATED MECHANISM FOR SUSPENSION AND DEALLOCATION OF COMPUTATIONAL THREADS OF EXECUTION IN A PROCESSOR		
First Named Inventor	KEVIN D. KISSELL		

INFORMATION DISCLOSURE STATEMENT TRANSMITTAL

Mail Stop **AMENDMENT**
Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Attached hereto is Form PTO-1449 listing documents believed relevant to the subject application. It is respectfully requested that the examiner review the information disclosed herein in detail, independently evaluate each item carefully in the consideration of the pending claims, and return an initialed copy of each form to the undersigned practitioner.

This disclosure statement should not be construed as a representation that a search has been made, that no other material information as defined in 37 CFR 1.56(a) exists, or as an admission that the information cited in the statement is, or is considered to be, material to patentability as defined in 37 CFR 1.56(b) or is available as a reference under 35 U.S.C. §102 *et seq.* Applicant reserves the right to swear behind or otherwise disprove the allege "prior" nature of any art cited should the facts support and the situation warrant such an action.

It is believed that this disclosure complies with the requirements of 37 CFR 1.56, 1.97, and 1.98, and the Manual of Patent Examining Procedures §609. If for some reason the examiner considers otherwise, it is respectfully requested that the undersigned be called so that any deficiencies can be remedied.

Some of the enclosed documents may have markings thereon. No significance is intended to be attached to the markings.

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Respectfully submitted,
HUFFMAN LAW GROUP
/James W. Huffman/
By: _____

JAMES W. HUFFMAN
Registration No. 35549
Tel: (719) 475-7103

10/31/2005
Date: _____

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Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary

Sheet 1 of 1

Complete if Known	
Application Number	10/684348
Filing Date	10/10/2003
First Named Inventor	Kevin D. Kissell
Group Art Unit	
Examiner Name	
Attorney Docket Number	MIPS.0189-00-US

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	AA	KISSELL, KEVIN D. "Microprocessor Forum (MPF) Conference Program Presentation: Architectural Extensions to the MIPS Architecture for High-Performance Embedded Systems." 15 October 2003.	
	AB	(webpage) Cray MTA-2 Historical Technical Papers, http://www.cray.com/products/programs/mta_2/resources.html. (12March 2005), (formerly http://www.cray.com/products/systems/mta/psdocs.html (7/2/2004)).	
	AC	ZASLAVSKY, LEONID et al. "A Scalable Approach for Solving Irregular Sparse Linear Systems on the Tera MTA Multithreaded Parallel Shared-Memory." Ninth SIAM Conference on Parallel Processing for Scientific Computing, San Antonio, TX. March 1999.	
	AD	SMITH, BURTON. "From Here to Petaflops." Keynote Address, Petaflops-systems Operations Working Review, (POWR), Bodega Bay, California, June 1998.	
	AE	BRIGGS, PRESTON. "Tuning the BLAS for the Tera." Workshop on Multithreaded Execution, Architecture and Compilation. (MTEAC 98), January 1998.	
	AF	ALVERSON, GAIL et al., "Scheduling on the Tera MTA." IPPS '95 Workshop on Job Scheduling Strategies for Parallel Processing, Santa Barbara, CA, April 1995, and in D.G.Feitelson and L. Rudolph, editors, Job Scheduling Strategies for Parallel Processing, Lecture Notes in Computer Science Vol. 949, pp. 19-44, Springer-Verlag 1995.	
	AG	SMITH, BURTON. "Folklore and Reality in High Performance Computing Slide Presentation." 1995	
	AH	SMITH, BURTON. "The Quest for General-Purpose Parallel Computing." 1994	
	AI	ALVERSON, GAIL et al. "Exploiting Heterogeneous Parallelism on a Multithreaded Multiprocessor." 6th ACM International Conference on Supercomputing, Washington DC, July 1992	
	AJ	CALLAHAN, DAVID. "Recognizing and Parallelizing Bounded Recurrences." Fourth Workshop on Languages and Compilers for Parallel Computing. Pp. 169-184. August 1991.	
	AK	CALLAHAN, DAVID et al. "Register Allocation via Hierarchical Graph Coloring." ACM SIGPLAN '91 Conference on Programming Language Design and Implementation, June 1991.	
	AL	ALVERSON, ROBERT. "Integer Division Using Reciprocals." 10th IEEE Symposium on Computer Arithmetic, June 1991.	
	AM	CALLAHAN, DAVID et al. "Improving Register Allocation for Subscripted Variables." ACM SIGPLAN Conference on Programming Language Design and Implementation, June 1990	
	AN	ALVERSON, ROBERT et al. "The Tera Computer System." ACM International Conference on Supercomputing, pp. 1-6, June 1990.	
	AO	SMITH, BURTON. "The End of Architecture." Keynote Address, 17th Annual Symposium on Computer Architecture, Seattle, Washington, May 1990	
	AP	ALVERSON, GAIL et al. "A Future-Based Parallel Language for a General Purpose Highly Parallel Computer." Languages and Compilers for Parallel Computing. Pp. 95-113, MIT Press, Cambridge, Massachusetts, 1990.	
	AQ	"MIT Alewife Project: Home Page." retrieved from URL: http://catfish.csail.mit.edu/alewife/ on 7/2/2004.	
	AR	ARVIND and R.A. INNAUCCI. "Two Fundamental Issues in Multiprocessing." In Proc. Of DFVLF-Conf. 1987 on Par.Proc.in Science and Eng., Bonn-Bad Godesberg, W. Germany, June 1987	

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.
[1] Applicant's unique citation designation number (optional). [2]Applicant is to place a check mark here if English language Translation is attached.
This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450**

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